

PROGRAMMABLE LOGIC DEVICE INCLUDING PROGRAMMABLE MULTI-  
GIGABIT TRANSCEIVERS

BACKGROUND OF THE INVENTION

TECHNICAL FIELD OF THE INVENTION

**[0001]** This invention relates generally to general-purpose integrated circuits and more particularly to programmable logic devices.

DESCRIPTION OF RELATED ART

**[0002]** Programmable devices are a class of general-purpose integrated circuits that can be configured for a wide variety of applications. Such programmable devices have two basic versions, mask programmable devices, which are programmed only by a manufacturer, and field programmable devices, which are programmable by the end-user. In addition, programmable devices can be further categorized as programmable memory devices or programmable logic devices. Programmable memory devices include programmable ready-only memory (PROM), erasable programmable read-only memory (EPROM) and electronically erasable programmable read-only memory (EEPROM). Programmable logic devices include programmable logic array (PLA) devices, programmable array logic (PAL) devices, erasable programmable logic devices (EPLD), and programmable gate arrays (PGA).

**[0003]** Field programmable gate arrays (FPGA) have become very popular for telecommunication applications, Internet applications, switching applications, routing applications, et cetera. Generally, an FPGA includes a programmable logic fabric and a programmable input/output section. The programmable logic fabric may be programmed to perform a wide variety of functions corresponding to the particular end-user applications. The programmable logic fabric may be implemented in a variety of ways. For example, the programmable logic fabric may be implemented in a systematic array configuration, a row base configuration, a sea-of-gates

configuration, or a hierarchical programmable logic device configuration.

**[0004]** The programmable input/output section is fabricated on the perimeter of a substrate supporting the FPGA and provides coupling to the pins of the integrated circuit package allowing users access to the programmable logic fabric. Typically, the programmable input/output section includes a number of serial/deserial transceivers to provide access to the programmable logic fabric. Such transceivers include a receiver section that receives incoming serial data and converts it into parallel data and a transmitter section that converts outgoing parallel data into an outgoing serial data stream.

**[0005]** Since FPGA's are used in a wide variety of applications, which are typically governed by one or more standards; the transceivers are programmed, to some degree, to support the appropriate standard. As such, the receiver section is programmed to convert serial data into parallel data and the transmitter section is programmed to convert parallel data into serial data in accordance with the same standard. This, however, provides a limitation in the use of an FPGA in that the transmit path and receive path must be coupled to the same device, or devices that conform to the same standard. Thus, using today's FPGA, if an application requires the FPGA to receive data from one device in accordance with a 1<sup>st</sup> standard and transmit process data to another device in accordance with a 2<sup>nd</sup> standard, the FPGA would have to dedicate 2 transceivers: 1 for the receiving of data and the other for the transmitting of data. In this example, the transmitter section of the 1<sup>st</sup> transceiver is always idle and the receiver section of the 2<sup>nd</sup> transceiver is always idle. In the heavily competitive integrated circuit market, having die area consumed by unused circuitry is extremely costly.

**[0006]** In addition, the transceivers of an FPGA are programmed in accordance with a particular standard being

supported by the FPGA. As such, each of the transceivers is programmed to support the same standard. As such, the devices to which the FPGA is coupled must also conform to the same standard. As such, the flexibility of usage of an FPGA is limited by requiring the environment in which it resides to utilize the same standard.

**[0007]** Further, the transceivers of the I/O section use a different clock domain than the programmable logic fabric. As the speed of the incoming and outgoing serial data increases well into the gigabit-per-second range, the separate clock domains of the input/output section and the programmable logic fabric are presenting synchronization issues between the two sections, resulting in corruption of data.

**[0008]** Therefore, a need exists for a universally programmable FPGA that provides universally programmable transceivers and further provides universal synchronization.

#### BRIEF SUMMARY OF THE INVENTION

**[0009]** The programmable logic device including programmable multi-gigabit transceivers of the present invention substantially meets these needs and others. In one embodiment, a programmable logic device includes a plurality of programmable multi-gigabit transceivers, programmable logic fabric, and a control module. Each of the plurality of programmable multi-gigabit transceivers is individually programmed to a desired transceiving mode of operation in accordance with a plurality of transceiver settings. The programmable logic fabric is operably coupled to the plurality of programmable multi-gigabit transceivers and is configured to process at least a portion of the data being transceived via the multi-gigabit transceivers. The control module is operably coupled to produce the plurality of transceiver settings based on a desired mode of operation for the programmable logic device. As such, via the transceiver settings, each of the multi-gigabit transceivers may be

programmed in accordance with a different standard such that the programmable logic device, which may be an FPGA, can communicate in a multi-standard environment.

**[0010]** In another embodiment, the programmable logic device includes a clock management module, a transmit physical media attachment (PMA) module, a receive physical media attachment (PMA) module, a transmit physical coding sub-layer (PCS) module, a receive physical coding sub-layer (PCS) module, and programmable logic fabric. The clock management module is operably coupled to provide a reference clock from one of a plurality of clock sources to the transmit PMA module and the receive PMA module.

**[0011]** The transmit PMA module generates a parallel transmit clock, the serial transmit clock and a transmit programmable logic clock based on the reference clock. The transmit PMA module provides the parallel transmit clock to the transmit PCS module and the transmit programmable logic clock to the programmable logic fabric. The programmable logic fabric utilizes the transmit programmable logic clock to produce transmit data words, which are provided to the transmit PCS module in accordance with parallel transmit clock and/or the transmit programmable logic clock. The transmit PCS module utilizes the parallel transmit clock to convert the transmit data words into parallel transmit data to provide the parallel transmit data to the transmit PMA module. The transmit PMA module utilizes the parallel and serial transmit clocks to convert the parallel transmit data into a transmit serial data stream.

**[0012]** The receive physical media attachment (PMA) module is operably coupled to generate a serial receive clock, a parallel receive clock, and a receive programmable logic clock. The receive PMA modules uses the serial receive clock and the parallel receive clock to convert serial received data into parallel receive data. The receive PMA module provides the parallel receive data to the receive physical coding sub-layer (PCS) module in accordance with the parallel

receive clock. The receive PCS module utilizes the parallel receive clock to convert the parallel received data into received data words and to provide the received data words to the programmable logic fabric. The programmable logic fabric utilizes the receive programmable logic clock to process the received data words. As such, synchronization is obtained throughout the programmable logic device.

**[0013]** An embodiment of a programmable multi-gigabit transceiver includes a programmable physical media attachment (PMA) module, a programmable physical coding sub-layer (PCS) module, a programmable interface, and a control module. The programmable PMA module is operably coupled to serialize high-speed output data in accordance with a programmed serialization setting and deserialize high-speed input data in accordance with a programmed deserialization setting to produce deserialized high-speed input data. The programmable PCS module is operably coupled to provide the high-speed output data to the programmable PMA module in accordance with a transmit PMA\_PCS interface setting and to receive the serialized high-speed input data from the programmable PMA module in accordance with a receive PMA\_PCS interface setting. The programmable interface operably couples the programmable PCS module to the programmable logic section in accordance with a programmed logic interface setting. The control module is operably coupled to generate the programmed serialization setting, the programmed deserialization setting, the receive PMA\_PCS interface setting, the transmit PMA\_PCS interface setting and the logic interface setting based on a desired mode of operation for the programmable multi-gigabit transceiver. With such a programmable transceiver, the transmit portion may be programmed in accordance with one standard while the receive section may be programmed in accordance with another standard.

**[0014]** Another embodiment of a programmable multi-gigabit transceiver includes a transmit section, a receive section, an interface, and a control module. The transmit section is

operably coupled to convert output data words into an output serial data stream in accordance with a transmit setting. The receive section is operably coupled to convert an input serial data stream into input data words in accordance with a receive setting. The interface is operably coupled to provide the output data words from a programmable logic section to the transmit section in accordance with the transmit setting and to receive the input data words from the receive section in accordance with the receive setting and provide them to the programmable logic section. The control module is operably coupled to produce the transmit setting and the receive setting based on transceiver operational requirements. Accordingly, the transmit section and receive section may be separately programmed based on desired operational parameters.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

**[0015]** Figure 1 is a schematic block diagram of a programmable logic device in accordance with the present invention;

**[0016]** Figure 2 is a schematic block diagram of a programmable multi-gigabit transceiver in accordance with the present invention;

**[0017]** Figure 3 is a schematic block diagram of an alternate embodiment of a programmable multi-gigabit transceiver in accordance with the present invention;

**[0018]** Figure 4 is a schematic block diagram of another embodiment of a programmable logic device in accordance with the present invention;

**[0019]** Figure 5 is a schematic block diagram of a programmable receive physical media attachment (PMA) module in accordance with the present invention;

**[0020]** Figure 6 is a schematic block diagram of a programmable transmit physical media attachment (PMA) module in accordance with the present invention;

**[0021]** Figure 7 is a schematic block diagram of a programmable receive physical coding sub-layer (PCS) module in accordance with the present invention;

**[0022]** Figure 8 is a schematic block diagram of a programmable transmit physical coding sub-layer (PCS) module in accordance with the present invention;

**[0023]** Figure 9 is a logic diagram of a method for programming a programmable multi-gigabit transceiver in accordance with the present invention;

**[0024]** Figure 10 is a logic diagram of an alternate method for programming a multi-gigabit transceiver in accordance with the present invention;

**[0025]** Figure 11 is a diagram illustrating the physical media attachment (PMA) mapping register in accordance with the present invention; and

**[0026]** Figures 12A through 12C illustrate various programming states for the programmable multi-gigabit transceivers in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

**[0027]** Figure 1 is a schematic block diagram of a programmable logic device 10 that includes programmable logic fabric 12, a plurality of programmable multi-gigabit transceivers (PMGT) 14-28 and a control module 30. The programmable logic device 10 may be a programmable logic array device, a programmable array logic device, an erasable programmable logic device, and/or a field programmable gate array (FPGA). When the programmable logic device 10 is a field programmable gate array (FPGA), the programmable logic fabric 12 may be implemented as a symmetric array configuration, a row-based configuration, a sea-of-gates configuration, and/or a hierarchical programmable logic device configuration. The programmable logic fabric 12 may further include at least one dedicated fixed processor, such as a microprocessor core or digital signal processor (DSP),

to further facilitate the programmable flexibility offered by a programmable logic device 10.

**[0028]** The control module 30 may be contained within the programmable logic fabric 12 or it may be a separate module in each of the MGTs. In either implementation, the control module 30 generates the control signals to program each of the transmit and receive sections of the programmable multi-gigabit transceivers 14-28. In general, each of the programmable multi-gigabit transceivers 14-28 performs a serial-to-parallel conversion on received data and performs a parallel-to-serial conversion on transmit data. The parallel data may be 8-bits, 16-bits, 32-bits, 64-bits, et cetera wide. Typically, the serial data will be a 1-bit stream of data that may be a binary level signal, multi-level signal, etc. Further, two or more programmable multi-gigabit transceivers may be bonded together to provide greater transmitting speeds. For example, if multi-gigabit transceivers 14, 16 and 18 are transceiving data at 3.125 gigabits-per-second, the transceivers 14-18 may be bonded together such that the effective serial rate is 3 times 3.125 gigabits-per-second.

**[0029]** Each of the programmable multi-gigabit transceivers 14-28 may be individually programmed to conform to separate standards. In addition, the transmit path and receive path of each multi-gigabit transceiver 14-28 may be separately programmed such that the transmit path of a transceiver is supporting one standard while the receive path of the same transceiver is supporting a different standard. Further, the serial rates of the transmit path and receive path may be programmed from 1 gigabit-per-second to tens of gigabits-per-second. The size of the parallel data in the transmit and receive sections, or paths, is also programmable and may vary from 8-bits, 16-bits, 32-bits, 64-bits, et cetera.

**[0030]** Figure 2 is a schematic block diagram of one embodiment of a representative one of the programmable multi-gigabit transceivers 14-28. As shown, the programmable

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deserialization setting 66 indicates the rate of the receive serial data 52, the desired rate of the receive parallel data 54, and the data width of the receive parallel data 54. The PMA memory mapped register 45, which will be described in greater detail with reference to Figure 11, may store the serialization setting 64 and the deserialization setting 66.

**[0032]** The programmable receive PCS module 42 and the programmable receive PCS module 42, which will be described in greater detail with reference to Figure 8, receives transmit data words 46 from the programmable transmit PCS module 42 and the programmable interface 36 and converts them into the transmit parallel data 48 in accordance with the transmit PMA\_PCS interface setting 60. The transmit data words 46, the size of the transmit parallel data words (e.g., 1-byte, 2-bytes, 3-bytes, 4-bytes, et cetera) and the corresponding transmission rate of the transmit parallel data 48. The programmable receive PCS module 44, which will be described in greater detail with reference to Figure 7, converts the received parallel data 54 into received data words 56 in accordance with the received PMA\_PCS interface setting 62. The received parallel data 54 setting 62 indicates the rate at which the received parallel data 54 will be received, the width of the parallel data 54, the transmit rate of the received data words 56 and the word size of the received data words 56.

**[0033]** The control module 35 also generates the logic interface setting 58 that provides the rates at which the transmit data words 46 and receive data words 56 will be transceived with the programmable logic fabric 12. Note that the transmit data words 46 may be received from the programmable logic fabric 12 at a different rate than the received data words 56 are provided to the programmable logic fabric 12.

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[0034] As one of average skill in the art will appreciate, each of the modules within the PMA module 32 and PCS module 34 may be individually programmed to support a desired data transfer rate. The data transfer rate may be in accordance with a particular standard, as those indicated in Figures 12A-12C, such that the receive path, i.e., the programmable receive PMA module 40 and the programmable receive PCS module 44 may be programmed in accordance with one standard while the transmit path, i.e., the programmable transmit PMA module 42 and the programmable transmit PCS module 38 may be programmed in accordance with another standard.

[0035] Figure 3 illustrates an alternate schematic block diagram of a representative one of the programmable multi-gigabit transceivers 14-28. In this embodiment, the programmable transmit PCS module 42. The receive section 70 includes the programmable receive PMA module 40 and the programmable receive PCS module 44. In this embodiment, the programmable receive PCS module 44, the control module 35 separately programs the transmit section and the receive section via transmit setting 74 and receive setting 76, respectively. The control module 35 also programs the programmable interface 36 via the logic interface setting 58. Accordingly, the control module 35 may program the receiver section 72 to function in accordance with one standard while programming the transmit section 70 in accordance with another standard. Further, the logic interface setting 58 may indicate that the programmable logic fabric 12 at a different rate than the received data words 56 are provided to the programmable logic fabric 12. As one of average skill in the art will appreciate, the programmable logic fabric 12 at a different rate include a transmit buffer and a receive buffer, and/or an

[0036] In this embodiment, the control module 35 respectively programs the transmit section and the receive section 72 via the logic interface setting 58. Accordingly, the control module 35 also programs the programmable interface 36 via the logic interface setting 58. The control module 35 may program the receiver section 72 to function in accordance with one standard while programming the transmit section 70 in accordance with another standard. Further, the logic interface setting 58 from the programmable logic fabric 12 at a different rate than the received data words 56 are received 58

elastic store buffer to facilitate the providing and receiving of the data words 46 and 56 to-and-from the programmable logic fabric 12.

**[0037]** Figure 4 is an alternate schematic block diagram of a programmable logic device 80. The programmable logic device 80 includes the programmable transmit PMA module 38, the programmable transmit PCS module 42, the programmable interface 36, the programmable logic fabric 12, the programmable receive PCS module 44, the programmable receive PMA module 40, and a clock management module 82. The clock management module 82 receives a plurality of clock sources 84 and provides one or more of them as a reference clock 86 to the programmable transmit PMA module 38 and the programmable receive PMA module 40. The plurality of clock sources 84 includes, but is not limited to, a low jitter external clock source, a recovered clock source as may be produced by the programmable receive PMA module 40, an internal clock of the programmable logic fabric 12, and/or a system clock. While the clock management module 82 in Figure 4 is shown to produce a single reference clock 86 that is provided to both the programmable transmit PMA module 38 and the programmable receive PMA module 40, the clock management module 82, in an alternative embodiment, may generate a separate transmit reference clock that is provided to the programmable transmit PMA module 38 and a separate receive reference clock that would be provided to the programmable receive PMA module 40.

**[0038]** The programmable receive PMA module 40, which will be described in greater detail with reference to Figure 5, receives the reference clock 86 and generates therefrom a serial receive clock 98. In addition, the programmable receive PMA module 40 generates a parallel receive clock 94 and a receive programmable logic clock 96 based on the reference clock 86 and/or the serial receive clock 98. The programmable receive PMA module 40 receives the serial data 52 and, after being initialized based on the reference clock 86, recovers the serial receive clock 98 therefrom. The

programmable receive PMA module 40 converts the receive serial data 52 into the receive parallel data 54 in accordance with the serial receive clock 98 and the parallel receive clock 94. The programmable receive PMA module 40 provides the parallel receive clock 94 to the programmable receive PCS module 44, which converts the receive parallel data 54 into the receive data words 56 in accordance with the parallel receive clock 94. The programmable receive PMA module 40 provides the receive programmable logic clock 96 to the programmable logic fabric 12, which processes the receive data words 56 in accordance with the receive programmable logic clock 96. Since the serial receive clock, the parallel receive clock, and the receive programmable logic clock are derived from the same reference clock, the conveyance of data between the programmable receive PMA module 40, the programmable receive PCS module 44, and the programmable logic fabric is synchronized.

**[0039]** Further details on the generation and use of the above clocks are described in co-pending patent application by Eric D. Groen et al. entitled MGT/FPGA CLOCK MANAGEMENT SYSTEM, having a filing date the same as the present patent application. This co-pending application is incorporated by reference, herein.

**[0040]** The programmable transmit PMA module 38 receives the reference clock 86 and produces therefrom a serial transmit clock 92. In addition, the programmable transmit PMA module 38 generates a transmit programmable logic clock 90 and a parallel transmit clock 88 from the serial transmit clock 92 and/or from the reference clock 86. The programmable transmit PMA module 38 provides the transmit programmable logic clock 90 to the programmable logic fabric 12, which processes data in accordance with the transmit programmable logic clock 90 to produce the transmit data words 46. The programmable transmit PMA module 38 provides the parallel transmit clock 88 to the programmable transmit PCS module 42, which converts the transmit data words 46 into

the transmit parallel data 48 in accordance with the parallel transmit clock 88. The programmable transmit PMA module 38 converts the transmit parallel data 48 into the transmit serial data 50 in accordance with the serial transmit clock 92 and the transmit parallel clock 88. The programmable PMA module 38 further utilizes the serial transmit clock 92 to transmit the transmit serial data 50. Since the serial transmit clock, the parallel transmit clock, and the transmit programmable logic clock are derived from the same reference clock, the conveyance of data between the programmable transmit PMA module 38, the programmable transmit PCS module 42, and the programmable logic fabric 12 is synchronized.

**[0041]** As one of average skill in the art will appreciate, the programmable transmit PMA module 38, the programmable transmit PCS module 42, the programmable interface 36, the programmable receive PCS module 44 and the programmable receive PMA module 40 may be programmed as described with reference to Figures 2 and/or 3.

**[0042]** Figure 5 illustrates a schematic block diagram of the programmable receive PMA module 40 that includes a programmable front-end 100, a data and clock recovery module 102, and a serial-to-parallel module 104. The programmable front-end 100 includes a receiver termination circuit 106 and a receiver amplifier 108. The data and clock recovery module 102 includes a data detection circuit 110 and a phase locked loop 112. The phase locked loop 112 includes a phase detection module 114, a loop filter 116, a voltage controlled oscillator 118, a 1<sup>st</sup> divider module 120, and a 2<sup>nd</sup> divider module 122.

**[0043]** The programmable front-end 100 is operably coupled to receive the receive serial data 52 and produce amplified and equalized receive serial data 124 therefrom. To achieve this, the receiver termination circuit 106 is programmed in accordance with a receive termination setting 126 to provide the appropriate termination for the transmission line between the programmable receiver PMA module 40 and the source that

originally transmitted the received serial data 52. The receive termination setting 126 may indicate whether the receive serial data 52 is a single-ended signal, a differential signal, may indicate the impedance of the termination line, and may indicate the biasing of the receiver termination circuit 106. For a more detailed discussion of the receiver termination circuit 106 refer to co-pending patent application by Charles W. Boecker et al. entitled RECEIVER TERMINATION NETWORK AND APPLICATION THEREOF and having the same filing date as the present application. This co-pending application is incorporated by reference, herein.

**[0044]** The receiver termination circuit 106 further biases the receive serial data 52 and provides the bias adjusted signal to the receiver amplifier 108. The gain and equalization settings of the receiver amplifier 108 may be adjusted in accordance with the equalization setting 128 and the amplification setting 130, respectively. The receiver amplifier 108 may be further described in co-pending patent application by William C. Black et al. entitled ANALOG FRONT-END HAVING BUILT-IN EQUALIZATION AND APPLICATIONS THEREOF and a filing date the same as the present patent application. This co-pending application is incorporated by reference, herein. Note that the receiver termination setting 126, the equalization setting 128, and the amplification setting 130 are part of the program deserialization setting 66 provided by the control module 35.

**[0045]** The data and clock recovery circuit 102 receives the amplified and equalized receive serial data 124 via the phase detection module 114 of phase locked loop 112 and via the data detection circuit 110. The phase detection module 114 has been initialized prior to receiving the amplified and equalized receive serial data 124 by comparing the phase and/or frequency of the reference clock 86 with a feedback reference clock produced by divider module 120. Based on this phase and/or frequency difference, the phase detection

module 114 produces a corresponding current that is provided to loop filter 116. The loop filter 116 converts the current into a control voltage that adjusts the output frequency of the voltage controlled oscillator 118. The divider module 120, based on a serial received clock setting 132 or settings within the bit stream, divides the output oscillation produced by the VCO 118 to produce the feedback signal. Once the amplified and equalized receive serial data is received, the phase detection module 114 compares the phase of the amplified and equalized receive serial data 124 with the phase of the amplified and equalized receive serial data 124. Based on a phase difference between the amplified and equalized receive serial data 124 and the feedback signal, a current signal is produced.

**[0046]** The phase detection module 114 provides the current signal to the loop filter 116, which converts it into a control voltage that controls the output frequency of the voltage controlled oscillator 118. At this point, the output of the voltage controlled oscillator 118 corresponds to a recovered clock 138. The recovered clock 138, which was referenced as the serial receive clock 98 in Figure 4, is provided to the divider module 122, the data detection circuit 110 and to the serial-to-parallel module 104. The data detection module 110 utilizes the recovered clock 138 to recover data 136 from the amplified equalized receive serial data 124. The divider module 122 divides the recovered clock 138, in accordance with a parallel receive and programmable logic clock setting 134, to produce the parallel receive clock 94 and the programmable logic receive clock 96. Note that the serial receive clock setting 132 and the parallel receive and programmable logic clock setting 134 are part of the programmable deserialization setting 66 provided to the programmable receive PMA module 40 by the control module 35.

**[0047]** The serial-to-parallel module 104, which may include an elastic store buffer, receives the recovered data 136 at a serial rate in accordance with the recovered clock

138. Based on a serial-to-parallel setting 135 and the parallel receive clock 194, the serial-to-parallel module 104 outputs the receive parallel data 54. The serial-to-parallel setting 135, which may be part of the programmable deserialization setting 66, indicates the rate and data width of the receive parallel data 54.

**[0048]** Figure 6 illustrates a schematic block diagram of a programmable transmit PMA module 38 that includes a phase locked loop 144, a parallel-to-serial module 140, and line driver 142. The phase locked loop 144 includes a phase detection module 146, a loop filter 148, a voltage control oscillator 150, a divider module 154, and a divider module 152.

**[0049]** The phase detection module 146 compares the phase and/or frequency of the reference clock 86 with the phase and/or frequency of a feedback oscillation produced by divider module 154. The phase detection module 146 generates a current signal to represent the phase and/or frequency difference between the reference clock 86 and the feedback oscillation. The loop filter 148 converts the current signal into a control voltage that regulates the output oscillation produced by the voltage control oscillator 150. Divider module 154, based on a serial transmit clock setting 158, divides the output oscillation of the VCO 150, which corresponds to the serial transmit clock 92, to produce the feedback oscillation. Note that the serial transmit clock setting 158 may be part of the programmed serialization setting 64 provided to the programmable transmit PMA module 38 by the control module 35. An embodiment of the VCO ISO is found in METHOD AND CIRCUIT FOR REDUCING VCO NOISE, by Eric D. Groen et al., and having the same filing date as the present application. This co-pending application is incorporated by reference, herein.

**[0050]** Divider module 152 receives the serial transmit clock 92 and, based on a parallel transmit and programmable logic clock setting 160, produces the parallel transmit clock

88 and the transmit programmable logic clock 90. The parallel transmit and programmable logic clock setting 160 may be part of the programmed serialization setting 64.

**[0051]** The parallel-to-serial module 140 receives the transmit parallel data 48 and produces therefrom a serial data stream 156. To facilitate the parallel-to-serial conversion, the parallel-to-serial module 140, which may include an elastic stored buffer, receives a parallel-to-serial setting 161 to indicate the width of the transmit parallel data 48 and the rate of the transmit parallel data, which corresponds to the parallel transmit clock 88. Based on setting 161, the serial transmit clock 92 and the parallel transmit clock 88, the parallel-to-serial module 140 produces the serial data stream 156 from the transmit parallel data 48.

**[0052]** The line driver 142 increases the power of the serial transmit data 156 to produce the transmit serial data 50. The line driver 142 may be programmed to adjust its pre-emphasis settings, slew rate settings, and drive settings via a pre-emphasis setting signal 162, a slew rate setting signal 164 and a drive setting signal 166. The pre-emphasis setting 162, slew rate setting 164 and drive setting 166 may be part of the programmed serialization setting 64. As one of average skill in the art will appreciate, while the diagram of Figure 6 is shown as a single-ended system, the entire system may be differential signaling and/or a combination of differential and single-ended signaling. Further details on the line driver 142 are described in co-pending patent application by Eric D. Groen et al. entitled DAC BASED DRIVER WITH SELECTABLE PRE-EMPHASIS SIGNAL LEVELS and having a filing date the same as the present patent application and in co-pending patent application by Eric D. Groen entitled TX LINE DRIVER WITH COMMON MODE IDLE STATE AND SELECTABLE SLEW RATES and having a filing date the same as the present patent application. These co-pending applications are incorporated by reference, herein.

**[0053]** Figure 7 is a schematic block diagram of a programmable receive PCS module 44 that includes a programmable data alignment module 170, a programmable descramble and decode module 172, a programmable storage module 174, and a programmable decode and verify module 176. The programmable data alignment module 170 includes a synchronous state machine 178, a value detect realign module 180, a block synchronization module 182, and a multiplexer 184. The programmable descramble and decode module 172 includes a 64b/66b descrambling module 188, an 8b/10b decoding module 186 and a multiplexer 190. The programmable storage module 174 includes a channel bonding module 194, an elastic storage buffer 192 and a multiplexer 196. The programmable decode and verify module 176 includes a receiver CRC (cycle redundancy check) module 200, a 64b/66b decoding module 198, and a multiplexer 202.

**[0054]** In operation, the programmable data alignment module 170 receives the receive parallel data 54. Based on the receive PMA\_PCS interface setting 62, the receive parallel data 54 may be passed via multiplexer 184 without processing, may be processed by the value detect realign module 180 and then passed via multiplexer 184 and/or further processed via the block synchronization module 182. As such, the setting 62 may bypass the programmable data align module 170, perform a value detection realignment and pass the realigned data and/or further utilize block synchronization, which is typically used for 10 gigabits-per-second signaling. The synchronization state machine 178 coordinates the alignment of the receive parallel data 54 via the value detect realign 180 and the block synchronization module 182. In addition, once the value detect realignment module 180 indicates that the data is valid and the block synchronization module 182 indicates that the PCS module is now in sync with the receive parallel data 54, the sync state machine 178 generates a lock signal.

**[0055]** The controls of the value detect realign module 180 include receiver polarity of the signal, alignment information, et cetera.

**[0056]** The programmable descramble and decode module 172 receives the output of multiplexer 184 and, based on setting 62, either passes the data via multiplexer 190 descrambles it via the 64b/66b descrambler 188 or decodes it via the 8b/10b decode module 186. The 64b/66b descrambling module 188 is described in greater detail in co-pending patent application by Joseph N. Kryzak et al. entitled FRAMING OF TRANSMIT ENCODED DATA AND LINEAR FEEDBACK SHIFTING and having a filing date the same as the present application. This co-pending application is incorporated by reference, herein. The 8b/10b decoding module 186 is further described in co-pending patent application by Joseph N. Kryzak et al. entitled ENHANCED 8B/10B ENCODING/DECODING AND APPLICATIONS THEREOF and having the same filing date as the present application. This co-pending application is incorporated by reference, herein.

**[0057]** The programmable storage module 174 may buffer the data it receives from multiplexer 190 via the elastic store buffer 192 to facilitate channel bonding or pass the data directly to multiplexer 196. The channel bonding module 194 enables the receiver of one programmable multi-gigabit transceiver to be linked or bonded with another receiver within another multi-gigabit transceiver to increase the effective serial data rate. The programmable storage module 174 is further described in co-pending patent application by Joseph N. Kryzak et al. entitled CHANNEL BONDING & CLOCK CORRECTION, WITH SYNC HEADERS, 64B/66B, MASTER SLAVE COMMUNICATIONS AND MASKING OF CBC SEQUENCES and having the same filing date as the present application. This co-pending application is incorporated by reference, herein.

**[0058]** The programmable decode and verify module 176 receives the output of multiplexer 196 and passes it directly as the receive data word 56 in accordance with setting 62, processes the data via a receive CRC module 200 and provides

that as the output, or decodes it via the 64b/66b decoding module 198. The 64b/66b decode module 198 is described in greater detail in co-pending patent application by Joseph N. Kryzak et al. entitled FRAMING OF TRANSMIT ENCODED DATA AND LINEAR FEEDBACK SHIFTING and having a filing date the same as the present application.

**[0059]** As one of average skill in the art will appreciate, the programmable receive PCS module 44 is readily programmable via settings 62 to decode the received parallel data 54 using a variety of decoding schemes, to process channel bonding, to verify and lock the incoming data, et cetera.

**[0060]** Figure 8 is a schematic block diagram of the programmable transmit PCS module 42 that includes a programmable verify module 210, a programmable encode module 212, a programmable storage module 214, and a programmable scramble module 216. The programmable verify module 210 includes a transmit CRC module 218 and a multiplexer 220. The programmable encode module 212 includes a 64b/66b encoding module 222, an 8b/10b encoding module 224, and a multiplexer 226. The programmable storage module 214 includes an elastic storage buffer 228 and a multiplexer 230. The programmable scramble module 216 includes a scramble module 232, a gearbox module 234, and a PMA converter 236.

**[0061]** The programmable verify module 210 is operably coupled to receive the transmit data words 46 and either pass them directly to the programmable encoding module 212 or perform a cycle redundancy check upon them. The transmit PMA\_PCS interface setting 60 indicates whether the transmit data words 46 will be directly passed to the programmable encode module 212 or be subject to a cycle redundancy check. The programmable encoding module 212, based on setting 60, either encodes the data received from the programmable verify module 210 via the 8b/10b encoder 224, the 64b/66b encoder 222 or passes the data directly to the programmable storage module 214. The 64b/66b encoder 222 is described in greater

detail with reference to co-pending patent application by Joseph N. Kryzak et al. entitled FRAMING OF TRANSMIT ENCODED DATA AND LINEAR FEEDBACK SHIFTING and having a filing date the same as the present application. The 8b/10b encoder 224 is more fully described in co-pending patent application by Charles W. Boecker et al. entitled ENHANCED 8B/10B ENCODING/DECODING AND APPLICATIONS THEREOF and having the same filing date as the present application. This co-pending application is incorporated by reference, herein.

**[0062]** The programmable storage module 214, based on setting 60, either passes the data that it receives from the programmable encode module 212 or stores it in the elastic storage buffer 228. The elastic storage buffer 228 allows for differing time rates between the transmit data words 46 and the transmit parallel data 48. For example, if the transmit data words 46 are 1-byte words at a rate of 500 megahertz and the transmit parallel data 48 is 2-bytes width at 300 megahertz, the data-per-cycle rate is different between the transmit data words 46 and the transmit parallel data 48. Accordingly, the elastic storage buffer 228 allows for data to accumulate in the elastic storage buffer and thus accommodate the differing data-per-rate discrepancies between the transmit data word 46 and the transmit parallel data 48.

**[0063]** The programmable scramble module 216 receives the output of multiplexer 230 and either passes it directly to the PMA converter 236 to produce the transmit parallel data 48 based on control signals or scrambles the data via the scramble module 232 and the gearbox module 234. The controls for the PMA converter 236 include polarity of the parallel data 48 and an indication of which path the data will be received from. The scramble module 232 and gearbox module 234 are further described in co-pending patent application by Joseph N. Kryzak et al. entitled FRAMING OF TRANSMIT ENCODED DATA AND LINEAR FEEDBACK SHIFTING and having the same filing date as the present application.

**[0064]** As one of average skill in the art will appreciate, the programmable transmit PCS module 42 may be programmed in a variety of ways to directly pass the transmit data words 46, encode them, scramble them, buffer them, et cetera. As such, with a wide diversity in programming abilities, the programmable transmit PCS module 42 as well as the entire programmable multi-gigabit transceiver may be programmed in accordance with many standards.

**[0065]** Figure 9 illustrates a logic diagram of a method for establishing the settings for the programmable multi-gigabit transceivers. Such a method may be performed by the control module 30 and/or control module 35. The process begins at Step 240 where a programming setting that indicates the desired mode-of-operation for the programmable multi-gigabit transceiver (PMGT) is received. The primitive may be received based on a user selection and/or based on an auto configuration process. Such an auto configuration process would sense the environment in which the PMGT is located to determine its operating mode. A primitive, which will be described in greater detail in Figures 12A-12C, generally indicates a particular application of a corresponding standard. For example, with reference to Figure 12A, the primitive GT10\_10GFC\_8 corresponds to the 10-gig fiber-channel standard that provides a serial transmission rate of 10.51875 gigabits-per-second, utilizes 64b/66b encoding and has a fabric interface of 64-bits data words at 159.37 megahertz.

**[0066]** Returning to the discussion of Figure 9, the process continues at Step 242 where the programming setting is converted into the programmed serialization setting, the programmed deserialization setting, the receive PMA\_PCS interface setting, the transmit PMA\_PCS interface setting and the logic interface setting. As previously mentioned, the primitive indicates the particular application of a standard. As such, the primitive will indicate the serial transmission rate, the corresponding encoding and the fabric interface

rate. Accordingly, based on these values, the settings, which program the PMGT are established.

**[0067]** The process then proceeds to Step 244 where the programmed serialization setting and the programmed deserialization setting are provided to the PMA memory mapped register. The PMA memory mapped register will be further described with reference to Figure 11. The process then proceeds to Step 246 where the transmit and receive PMA\_PCS interface settings and the programmable logic interface settings are provided to the PCS register. Once the settings are stored in the appropriate registers, the PMA sections of the PMGT and the PCS sections of the PMGT are correspondingly programmed as described in Figures 5-8.

**[0068]** Figure 10 is a logic diagram of a method that further indicates the programming of the programmable MGT by control module 30 and/or control module 35. The process begins at Step 250 where the programmed serialization setting is generated to enable, logically disable and/or physically disable at least one element of the programmable PMA receiver module. For example, with reference to Figure 5, the programmed serialization setting 66 may be used to enable and/or disable the programmable front-end 100, the phase locked loop 112, the data detection circuit 110 and/or the serial-to-parallel module 104. The elements to be disabled are based on the particular mode-of-operation. If data is not being received, the entire programmable received PMA module may be disabled thus conserving power.

**[0069]** Returning to the discussion of Figure 10, the process proceeds to Step 252 where the programmed deserialization setting is generated to enable, logically disable or physically disable at least one element of the programmable PMA transmitter module. For example, with reference to Figure 6, the programmed serialization setting 64 may enable or disable physically (i.e., remove power there from) or logically disable (i.e., logically hold an input or

output to a known state) the phase locked loop 144, the parallel-to-serial module 140, and/or the line-driver 142.

**[0070]** Returning to the discussion of Figure 10, the process then proceeds to Step 254 where the transmit PMA\_PCS interface setting is generated to enable, logically disable and/or physically disable at least one element of the programmable PCS transmit module. The process then proceeds to Step 256 where the received PMA\_PCS interface setting is generated to enable, logically disable and/or physically disable at least one element of the programmable PCS received module. The elements of the programmable PCS transmit module are shown in Figure 8 and the elements of the programmable receive PCS module are shown in Figure 7.

**[0071]** Figure 11 illustrates the contents of the PMA mapping register 45. As shown, the mapping register includes memory spaces for indicating a variety of operations for the PMA module including a master bias, transmit divider ratio, transmit loop filter settings, transmit mode control, transmit output level, transmit output mode, receive divider ratio, receive loop filter settings, received mode of operation, received forward error encoding and power control of the PMA module.

**[0072]** Figures 12A-12C illustrate a plurality of primitives, their corresponding standards, serial rate, encoding scheme and fabric interface rate. Accordingly, any of these primitives, or programming settings, may be selected by a user of the device and the corresponding settings derived to program the programmable logic device to support the particular standard.

**[0073]** The preceding discussion has presented a programmable logic device that includes programmable multi-gigabit transceivers. The multi-gigabit transceivers have separately programmable transmit paths and receive paths and may be independently programmed from one another within the programmable logic device. As such, a great deal of flexibility is provided via such a programmable logic device.

As one of average skill in the art will appreciate, other embodiments may be derived from the teaching of the present invention without deviating from the scope of the claims.